

**WHAT IS CLAIMED IS :**

1. A period control circuit for self-refresh operation in a semiconductor memory device comprising:

pulse generating means for outputting a predetermined  
5 periodic pulse train responding to an external control signal;

frequency-dividing means for outputting a number of pulse  
trains which have different periods from each other by frequency-  
dividing said pulse train output from said pulse generating means;

at least one temperature detecting means for outputting a  
10 temperature detection signal by detecting that the ambient  
temperature of said memory device reaches at a predetermined  
level;

at least one voltage detecting means for outputting a voltage  
detection signal by detecting that the power supply voltage  
15 applied to said memory device reaches at a predetermined level;  
and

pulse selecting means for outputting a self-refresh master  
clock by selecting one of said pulse trains responding to said  
voltage detection signal and said temperature detection signal.

20 2. A period control circuit for self-refresh operation in a  
semiconductor memory device comprising:

pulse generating means for outputting a predetermined  
periodic pulse train responding to an external control signal;

frequency-dividing means for outputting a number of pulse  
25 trains which have different periods from each other by frequency-  
dividing said pulse train output from said pulse generating means;

at least one temperature detecting means for outputting a  
temperature detection signal by detecting that the ambient  
temperature of said memory device reaches at a predetermined  
30 level;

at least one voltage detecting means for outputting a voltage  
detection signal by detecting that the power supply voltage

applied to said memory device reaches at a predetermined level;

combination pulse train generating means for outputting a number of combination pulse trains by combining the said pulse trains output from said frequency-dividing means; and

- 5 pulse selecting means for outputting a self-refresh master clock by selecting one of said combination pulse trains responding to said voltage detection signal and said temperature detection signal.